WHAT IS CLAIMED IS:

1. A system on a chip (SOC) processor for multimedia, comprising:

a pre-processor that converts an external image signal into a compressible signal;

an encoder/decoder that generates compressed data by compressing the compressible signal, and codes the compressed data to produce a coded image signal;

a post-processor that converts the coded image signal into a format for use by an image displaying apparatus;

a graphic accelerator that processes three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus;

a first system bus coupled to the encoder/decoder circuit unit; and

a second system bus coupled between the pre-processor, the post-processor, and the graphic accelerator,

wherein the first system bus and the second system bus communicate data to each other through a bridge DMA circuit unit, and a controller controls said pre-processor, said encoder/decoder, said post-processor and said graphic accelerator.

2. The SOC processor of claim 1, wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus.

3. The SOC processor of claim 1, wherein the graphic accelerator comprises:

a geometry computation unit that performs geometry computation to display an object on the image displaying apparatus; and

a rendering computation unit that performs rendering computation for visual representation of the object displayed on the image displaying apparatus with at least one of color, brightness and a design.

4. The SOC processor of claim 3, further comprising a texture/pixel cache configured to store 2-dimensional information of an object to be displayed and remove hidden surfaces of the image signal after three dimensional graphic processing.

5. The SOC processor of claim 4, further comprising a buffer coupled between the controlling unit and the first system bus, wherein the buffer is capable of storing data for graphic to support the graphic accelerator.

6. The SOC processor of claim 5, wherein the buffer is implemented by using a static random access memory (SRAM) with a dual porter.

7. The SOC processor of claim 5, wherein the buffer can receive data from an external memory having geometry information.

8. The SOC processor of claim 7, wherein the external memory is a synchronous dynamic random access memory (SDRAM) having a clock speed synchronized with that of the controlling unit.

9. The SOC processor of claim 7, wherein the graphic accelerator receives the stored information by directly accessing the buffer.

10. A method of performing multimedia processing on a system on a chip (SOC), comprising the steps of:

converting an external image signal into a compressible signal;

compressing the compressible signal to generate compressed data, and coding the compressed data to produce a coded image signal;

converting the coded image signal into a format for use by an image displaying apparatus; and

processing three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus;

wherein said compressing is performed in a circuit coupled to a first system bus, and said converting steps and said processing step are performed in a circuit coupled to a second system bus, such that said first system bus and said second system bus can operate at different respective clock frequencies, and

wherein said first system bus and said second system bus communicate data to each other through a bridge DMA circuit unit, and a controller controls said converting steps, said compressing step, and said processing step.

11. The method of claim 10, wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus.

12. The method of claim 10, wherein the processing comprises:

performing geometry computation to display an object on the image displaying apparatus; and

performing rendering computation for visual representation of the object displayed on the image displaying apparatus with at least one of color, brightness and a design.

13. The method of claim 12, further comprising storing 2-dimensional information of an object to be displayed, and removing hidden surfaces of the image signal after three dimensional graphic processing.

14. The method of claim 13, further comprising storing graphic data in a buffer to support the processing step.

15. The method of claim 14, wherein the buffer is implemented by using a static random access memory (SRAM) with a dual porter.

16. The method of claim 14, wherein the buffer receives data from an external memory having geometry information.

17. The method of claim 16, wherein the external memory is a synchronous dynamic random access memory (SDRAM) having a clock speed synchronized with that of the controlling unit.

18. The method of claim 16, wherein the stored information is received in a graphic accelerator for processing by directly accessing the buffer.

19. A computer readable medium configured for storing instructions to perform multimedia processing on a system on a chip (SOC), said instructions comprising:

converting an external image signal into a compressible signal;

compressing the compressible signal to generate compressed data, and coding the compressed data to produce a coded image signal;

converting the coded image signal into a format for use by an image displaying apparatus; and

processing three-dimensional graphic computation with respect to the image signal output on the image displaying apparatus;

wherein said compressing is performed in a circuit coupled to a first system bus, and said converting instructions and said processing instruction are performed in a circuit coupled to a second system bus, such that said first system bus and said second system bus can operate at different respective clock frequencies, and

wherein said first system bus and said second system bus communicate data to each other through a bridge DMA circuit unit, and a controller controls said converting instructions, said compressing instruction, and said processing instruction.

20. The computer readable medium of claim 19, wherein a clock frequency of the first system bus is higher than a clock frequency of the second system bus.